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(54) VIDEO SIGNAL ENCODING MULTIPLEXER

(57) Abstract

Objective: To provide an effective control means with good rate allocation to individual channels by using an amount encoded for a previous prescribed period in a device that respectively encodes video signals of several channels using several video signal encoding circuits, respectively, temporarily stores them in several buffer memories, and reads out and multiplexes them at a prescribed rate.

Constitution: Several video signal encoding circuits for encoding video signals of several channels, buffer

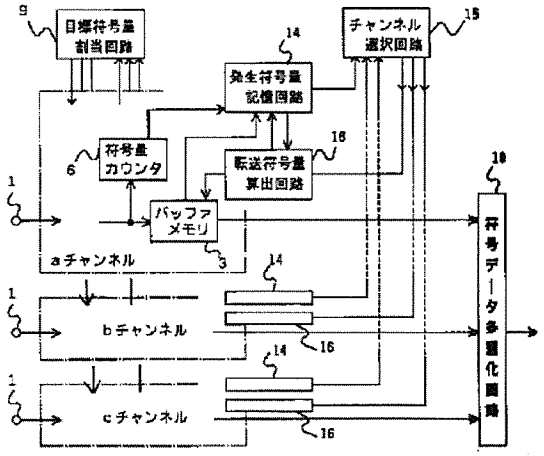

Figure 1

memories of individual channels for temporarily storing the encoded data, encoded quantity storage circuits for storing data such as the amount of data for a previous prescribed time, and a channel selecting circuit for selecting the channel having the oldest data such as the amount encoded among all the channels are installed. From the buffer memory of the channel having the oldest data such as the amount encoded, the encoded data are sequentially read out and output.

Key:

a	Channel
b	Channel
c	Channel
3	Buffer memory
6	Encoded quantity counter
9	Target encoding quantity allocating circuit
10	Encoded data multiplexing circuit
14	Encoded quantity storage circuit
15	Channel selecting circuit
16	Transferred encoded quantity calculating circuit

Claims

1. A video signal encoding multiplexer, characterized by the fact that a video signal encoding multiplexer having several video signal encoding circuits for encoding video signals of several channels for each channel, several buffer memories for temporarily storing the encoded data generated in each video signal encoding circuit for each channel, and an encoded data multiplexing circuit for multiplexing the encoded data that are read at a prescribed rate out of each buffer memory, it is equipped with several encoded quantity storage circuits having memories for storing of the amount encoded for a prescribed period in each video signal encoding circuit and/or the last encoded data storage addresses stored in the buffer memories as well as the time number showing the relative time of the prescribed period, a channel selecting circuit that selects the channel with the oldest time number or the channel having the largest total amount encoded in the buffer memories of two or more channels with the oldest time number from the time number stored in each encoded quantity storage circuit, and a transferred encoded quantity calculating circuit for outputting the encoded amount gt calculated and selected by a selecting signal from the channel selecting circuit and an encoded data readout control signal; and the buffer memories of each channel are controlled by the encoded amount gt or the storage addresses and the encoded data readout control signal.

2. The video signal encoding multiplexer of Claim 1, characterized by the fact that the encoded quantity storage circuit is equipped with a memory that stores a time number showing the relative time of the amount encoded for a prescribed time in the video signal encoding circuit and said prescribed time and the last encoded data storage address stored in the buffer memory; and a memory that temporarily stores the oldest amount encoded g0 and the oldest time number t0 stored in the above-mentioned memory and the last encoded data storage address b0.

3. The video signal encoding multiplexer of Claims 1 and 2, characterized by the fact that the transferred encoded quantity calculating circuit receives the selecting signal from the channel selecting circuit and outputs the encoded amount gt calculated and selected from the amount encoded g0 from the encoded quantity storage circuit and a preset fixed amount gMAX of encoding or the storage address b0 from the temporary storage memory and the code readout control signal to the buffer memory of the corresponding channel.

4. The video signal encoding multiplexer of Claims 1 and 2, characterized by the fact that the transferred encoded quantity calculating circuit receives the selecting signal from the channel selecting circuit and calculates the amount encoded gt by gt = g0 if g0 < gMAX and gt = gMAX – gMIN if g0 ≥ gMAX, when the amount encoded g0 from the encoded quantity storage circuit and the preset fixed amounts gMAX and gMIN of encoding are calculated and selected.

5. The video signal encoding multiplexer of Claims 1 and 2, characterized by the fact that the transferred encoded quantity calculating circuit receives the selecting signal from the channel selecting circuit and calculates a storage address bt, in which the last encoded data are stored, by b0' = b0 if br < b0 and b0' = b0 + B if br > b0, bt' = b0' if b0' < b'MAX (= br + gMAX) and bt' = b'MAX – gMIN if b0' > b'MAX, and bt = bt' if bt' < B and bt = bt' – B if bt' > B, when the amount encoded g0 from the encoded quantity storage circuit, preset fixed amounts gMAX and gMIN of encoding, a readout address br as a starting point of the encoded data storage of the buffer memory of the channel, a storage address b0 in which the oldest and the last encoded data are stored, and a storage capacity B of the buffer memory are calculated and selected.

6. The video signal encoding multiplexer of Claim 1, characterized by the fact that it is equipped with an IP synchronous control circuit that repeatedly outputs an encoded data P signal in which a differential signal, wherein the motion of images of two continuous screens is corrected, is encoded and an encoded data I signal, in which video signals of all images are encoded, at a prescribed field period Fg and controls the timing for outputting the encoded data I signal of each channel so that the timings are shifted from each other.

Detailed explanation of the invention

[0001]

Industrial application field

The present invention pertains to a video signal encoding multiplexer that encodes and multiplexes video signals of several channels.

[0002]

Prior art

Recently, in the storage media (media such as software and data using tapes or disks) field and the communications field, studies on international standardization concerning high-efficiency encoding of dynamic video signals have been advanced. Figure 12 shows the constitution of a representative video signal encoder of the prior art that is used for high-efficiency encoding of dynamic video signals. In Figure 12, video signals provided to an input terminal 1 of a video signal encoder are converted into encoded data by an encoding circuit 2 and output to a buffer memory 3 and an encoded quantity counter 6. The encoded data input into the buffer memory 3 are stored in the buffer memory 3, read out at a prescribed fixed rate from the buffer memory 3, output to an output terminal 4, and transmitted to a transmission system. On the other hand, the encoded quantity counter 6 into which the encoded data are input from the encoding circuit 2 counts the encoded data and outputs to a complexity calculating circuit 5 the encoded amount of the encoded data in the current field obtained by counting. The complexity calculating circuit 5 calculates the complexity X of the video signals of the current field from the amount encoded in the current field input from the encoded quantity counter 6 and a quantization step (a parameter for adjusting the amount encoded; hereinafter, it is assumed that the amount encoded is decreased with an increase in this value) used in encoding of the current field output from the encoding circuit 2 and outputs it to a quantization step calculating circuit 7.

[0003]

In addition, the above-mentioned encoded quantity counter 6 counts the total amount encoded in the buffer memory 3 apart from the amount encoded in the above-mentioned current field from the input encoded data, stores it, and outputs the total amount encoded in said buffer memory 3 to the quantization step calculating circuit 7. As a result, the quantization step calculating circuit 7 calculates a target encoding amount to be generated in the next field and a quantization step value to be used for the target amount by calculating using the total amount encoded in the buffer memory 3 from the encoded quantity counter 6, the complexity X calculated by the above-mentioned complexity calculating circuit 5, and a fixed rate value Rt of the transmission system, which is provided from a separate transmission rate designating terminal 8, and outputs them to the encoding circuit 2. In other words, if images are complicated and the amount encoded seems to be large or if a large encoded amount is stored in the buffer memory 3, the quantization step calculating circuit 7 reduces the encoded amount of the encoding circuit 2 and outputs a large quantization step to recover a normal state. The encoding circuit 2 is then reset by the attained quantization step value, and encoding of the next field is started. Thereafter, the encoding is similarly repeated.

[0004]

The application of this video signal encoder to broadcasting systems is progressing, but unique requests in are found broadcasting systems. One of them is that in broadcasting systems, it is often necessary to simultaneously transmit several video signals if a large accident occurs, etc. For this reason, in a broadcasting system such as a FPU (Field Pick Up) device with a limited number of channels, a video signal encoding multiplexer that divides a given transmission system of 15 Mbps, for instance, by 3 into 5 Mbps each, prepares 3 units of the above-mentioned video signal encoders with the same number of channels, and applies time-division multiplexing to encoded data generated from each video signal encoder has been proposed.

[0005]

On the other hand, in a video signal encoding multiplexer, if video signals with complicated patterns are encoded by the same quantization step as that of video signals with uncomplicated patterns, since a quantization step that increases the encoded amount of the video signals with complicated patterns is employed for the encoding, the encoded amount of the video signals with uncomplicated patterns is increased. Therefore, if the transmission rate for transmitting the encoded data is fixed, the picture quality must be decreased by raising the quantization step for complicated patterns and encoding and transferring the video signals so that the amount encoded does not exceed the transmission rate. Conversely, for simple patterns, since the amount encoded is deficient, the picture quality is raised by lowering the quantization step more than is necessary, and the video signals are encoded and transmitted. As mentioned above, in a conventional video signal encoding multiplexer, since the transmission rate of each channel is respectively fixed at a fixed value, the picture quality of a channel that sends complicated patterns is poor, and the picture quality of a channel of simple patterns is enhanced, so variation of the picture quality between the respective channels results.

[0006]

As a method to solve this problem, the following method has been considered. In other words, if the number of channels is 3, a target amount Tch of code for each channel (individual target encoding amount) is allocated in accordance with the complexities Xa, Xb, and Xc of the images of each channel according to the following equation.

$$Tch = (Xch/(Xa + Xb + Xc) \times Rt \qquad (1)$$

Where, Xch: complexity of a certain channel

ch: channel numbers a, b, and c

Rt: fixed rate value of the transmission system

In addition, an individual Rch = Tch that can transmit the same encoded amount as the individual target encoding amount Tch is allocated to the transmission rate (individual rate) Rch of each channel.

[0007]

Figure 13 shows a video signal encoding multiplexer, and in this constitution, a target encoding quantity allocating circuit 9 and an encoded data multiplexing circuit 10 for multiplexing are added to several video signal encoders shown in Figure 12. In Figure 13, the target encoding quantity allocating circuit 9 is for attaining the individual rate Rch according to equation (1). The output of the individual rate Rch attained in this circuit is input into the above-mentioned transmission rate designating terminal 8 of each channel of Figure 12, and the amount encoded is adjusted by the complexity of images of each channel. In addition, the target encoding quantity allocating circuit 9 simultaneously controls the buffer memories 3 of each channel and reads out encoded data corresponding to the size of the individual rate Rch from each buffer memory 3. The encoded data read out of each buffer memory 3 are output to the encoded data multiplexing circuit 10, and a code (header) required for transmission is added to them by the encoded data multiplexing circuit 10, and they are multiplexed, output, and transmitted to the transmission system.

[0008]

Figure 14 schematically shows changes in the amount encoded in buffer memories at the transmission side and reception side in a case in which video signals of 2 channels are multiplexed and transmitted using the video signal encoding multiplexer shown in Figure 13. The above-mentioned schematic diagram shows a case in which it is assumed that an encoder (encoding circuit) and buffer memories of 2 fields exist at the transmission side and a decoder and buffer memories of 2 fields exist at the reception side (may be a general decodable device, not shown in the figure). In Figure 14, double line frames 11 at the transmission side are encoded parts that are generated from the encoder (encoding circuit) for the current one field period, double line frames 12 at the reception side are image encoded parts that are decoded and output by the decoder for the current one field period, and frames in a transmission system 13 as an intermediate area are encoded parts that are transmitted for the current one field period. In addition, for simplicity, the amount encoded shows one block indicated with a square as a unit.

In addition, the transmission rate value after changing the individual rate is shown in ( ) at a block unit.

[0009]

Figure 14(a) shows a stable state in which both channel a and channel b are transmitted at the same transmission rate. In other words, the fourth field starts encoding for the current one field period at the transmission side, the second field starts the transmission for the current one field period of the transmission system, and the 0^{th} field starts decoding for the current one field period at the reception side. Each operation is finished at the end of this one field period. Figure 14(b) shows a case in which the encoded amount of the fifth field is increased by 1.5 times in channel a at the transmission side and the encoded amount of the fifth field is reduced to 1/2 in channel b. If this state is continued thereafter, the transmission rate of each channel of the next field is reset to a new individual rate attained from the complexity Xa of images of the fifth field of channel a.

[0010]

In other words, as shown in Figure 14(c), the transmission rate of channel a at the transmission side is increased to 3 blocks in the sixth field, which is the same as that of the fifth field, and encoded data of 1.5 fields are transmitted for one field period. In addition, the transmission rate of channel b is decreased to 1 block, and encoded data of 0.5 field are transmitted for one field period. In this manner, the transmission rate of each channel is changed in accordance with the complexity of input images, so a multiplexed transmission with minimal variation of the picture quality in which the fixed rate Rt of the transmission system is effectively utilized can be realized.

[0011]

On the other hand, the third field part at the transmission side of Figure 14(a) corresponds to a marginal field that is stored in the buffer memory at the transmission side to prevent the generation of erroneous operations due to a shortage in the transmitted encoded amount, when the encoded amount of the second field is smaller than the target encoding amount. Conversely, the first field part at the reception side corresponds to a marginal field that is stored in the buffer memory at the reception side to prevent erroneous operations in which images cannot be output for the next field period, when the encoded amount of the second field is so large that transmission cannot be completed for one field period. Therefore, marginal fields are required to prevent erroneous operations of the video signal encoder.

[0012]

However, in the video signal encoding multiplexer shown in Figure 13, if the stable state after changing the transmission rate allocation shown in Figure 14(d) is passed through, the marginal field disappears completely in channel b at the reception side as shown in Figures 14(a) and (f). Therefore, if the encoded amount of the fifth field, for instance, in channel b is even slightly larger than the target encoding amount, the encoded data cannot be completely sent for one field period at the stage of Figure 14(d), and encoded data that are input into the decoder at the reception side for one field period of Figure 14(f) are deficient. For this reason, the marginal field at the reception side must be further increased by one field.

[0013]

Problems to be solved by the invention

In the above-mentioned explanation, a case in which the ratio of the amount encoded between the channels is 1:3 has been explained. However, in a conventional video signal encoding multiplexer, if the ratio of the amount encoded is further increased, further marginal fields must be added, and marginal fields at the reception side must be increasingly added. However, by adding marginal fields, not only is a large-scale circuit for increasing the storage capacity of the buffer memories required, but a transmission delay for a period of several fields due to the encoded data residing in the buffer memories is generated. In order to solve the above-mentioned problems, the objective of the present invention is to provide a video signal encoding multiplexer that distributes individual rates by using the amount actually encoded for a previous prescribed period, for example, one field period, instead of a target encoding amount for each channel or the complexity of images.

[0014]

Means to solve the problems

In order to achieve the above-mentioned objective, the present invention provides a video signal encoding multiplexer characterized by the fact that a video signal encoding multiplexer having several video signal encoding circuits for encoding video signals of several channels for each channel, several buffer memories for temporarily storing the encoded data generated in each video signal encoding circuit for each channel, and an encoded data multiplexing circuit for multiplexing the encoded data that are read at a prescribed rate out of each buffer memory, is equipped with several encoded quantity storage circuits having memories for storing the amount encoded for a prescribed period in each video signal encoding circuit and/or the last encoded data storage addresses stored in the buffer memories as well as a time number showing the relative time of the prescribed period, a channel selecting circuit that selects the channel with the

oldest time number or the channel having the largest total amount encoded in the buffer memories of two or more channels with the oldest time number from the time number stored in each encoded quantity storage circuit, and a transferred encoded quantity calculating circuit for outputting the encoded amount gt calculated and selected by a selecting signal from the channel selecting circuit and an encoded data readout control signal; and the buffer memories of each channel are controlled by the amount encoded gt or the storage addresses and the encoded data readout control signal.

[0015]

In addition, the present invention provides a video signal encoding multiplexer characterized by the fact that the encoded quantity storage circuit is equipped with a memory that stores a time number showing the relative time of the amount encoded for a prescribed time in the video signal encoding circuit and said prescribed time and the last encoded data storage address stored in the buffer memory; and a memory that temporarily stores the oldest amount encoded g0 and the oldest time number t0 stored in the above-mentioned memory and the last encoded data storage address b0.

[0016]

Moreover, the present invention provides a video signal encoding multiplexer characterized by the fact that the transferred encoded quantity calculating circuit receives the selecting signal from the channel selecting circuit and outputs the encoded amount gt calculated and selected from the amount encoded g0 from the encoded quantity storage circuit and a preset fixed amount gMAX of encoding or the storage address b0 from the temporary storage memory and the code readout control signal to the buffer memory of the corresponding channel.

[0017]

Furthermore, the present invention provides a video signal encoding multiplexer characterized by the fact that the transferred encoded quantity calculating circuit receives the selecting signal from the channel selecting circuit and calculates the amount encoded gt by $gt = g0$ if $g0 < gMAX$ and $gt = gMAX - gMIN$ if $g0 \geq gMAX$, when the amount encoded g0 from the encoded quantity storage circuit and the preset fixed amounts gMAX and gMIN of encoding are calculated and selected.

[0018]

In addition, the present invention provides a video signal encoding multiplexer characterized by the fact that the transferred encoded quantity calculating circuit receives the

selecting signal from the channel selecting circuit and calculates the storage address bt, in which the last encoded data are stored, by b0' = b0 if br < b0 and b0' = b0 + B if br > b0, bt' = b0' if b0' < b'MAX (= br + gMAX) and bt' = b'MAX – gMIN if b0' > b'MAX, and bt = bt' if bt' < B and bt = bt' – B if bt' > B, when the amount encoded g0 from the encoded quantity storage circuit, preset fixed amounts gMAX and gMIN of encoding, a readout address br as a starting point of the encoded data storage of the buffer memory of the channel, a storage address b0 in which the oldest and the last encoded data are stored, and a storage capacity B of the buffer memory are calculated and selected.

[0019]

Moreover, the present invention provides a video signal encoding multiplexer characterized by the fact that it is equipped with an IP synchronous control circuit that repeatedly outputs an encoded data P signal in which a differential signal, wherein the motion of images of two continuous screens is corrected, is encoded and an encoded data I signal, in which video signals of all images are encoded, at a prescribed field period Fg and controls the timing for outputting the encoded data I signal of each channel so that the timings are shifted from each other.

[0020]

Operation of the invention

The operation of the present invention is as follows. In encoding video signals, a time number showing the relative time of at least one of the amount encoded for a prescribed period or the last encoded data storage addresses stored in the buffer memories and the prescribed period is stored in an encoded quantity storage circuit, and the channel with the oldest time number or the channel having the largest total amount encoded in the buffer memories of two or more channels with the oldest time number from the time number stored in each encoded quantity storage circuit is selected by the channel selecting circuit. From the transferred encoded quantity calculating circuit, the encoded amount gt calculated and selected by a selecting signal and an encoded data readout control signal are output, and the amount encoded gt or the storage addresses and the encoded data readout control signal are generated to control the buffer memories of each channel.

[0021]

In addition, the amount encoded for a prescribed time in the video signal encoding circuit and a time number showing the relative time of said prescribed time and the last encoded data storage address stored in the buffer memory are stored in the memory of the encoded quantity

storage circuit, and the oldest amount encoded g0 and the oldest time number t0 stored in the above-mentioned memory and the last encoded data storage address b0 are stored in a temporary storage memory. Moreover, after receiving the selecting signal from the channel selecting circuit, the transferred encoded quantity calculating circuit outputs the encoded amount gt calculated and selected from the amount encoded g0 from the encoded quantity storage circuit and a preset fixed amount gMAX of encoding or the storage address b0 from the temporary storage memory and the code readout control signal to the buffer memory of the corresponding channel.

[0022]

Furthermore, after receiving the selecting signal from the channel selecting circuit, when the amount encoded g0 from the encoded quantity storage circuit and preset fixed amounts gMAX and gMIN of encoding are calculated and selected, the transferred encoded quantity calculating circuit calculates the amount encoded gt by $gt = g0$ if $g0 < gMAX$ and $gt = gMAX - gMIN$ if $g0 \geq gMAX$.

[0023]

In addition, after receiving the selecting signal from the channel selecting circuit, when the amount encoded g0 from the encoded quantity storage circuit, preset fixed amounts gMAX and gMIN of encoding, a readout address br as a starting point of the encoded data storage of the buffer memory of the channel, a storage address b0 in which the oldest and the last encoded data are stored, and a storage capacity B of the buffer memory are calculated and selected, the transferred encoded quantity calculating circuit calculates the storage address bt, in which the last encoded data are stored, by $b0' = b0$ if $br < b0$ and $b0' = b0 + B$ if $br > b0$, $bt' = b0'$ if $b0' < b'MAX$ (= br + gMAX) and $bt' = b'MAX - gMIN$ if $b0' > b'MAX$, and $bt = bt'$ if $bt' < B$ and $bt = bt' - B$ if $bt' > B$.

[0024]

Moreover, the IP synchronous control circuit repeatedly outputs an encoded data P signal in which a differential signal, wherein the motion of images of two continuous screens is corrected, is encoded and an encoded data I signal, in which video signals of all images are encoded, at a prescribed field period Fg and controls the timing for outputting the encoded data I signal of each channel so that the timings are shifted from each other.

[0025]

Application examples

Application Example 1

A first application example of the present invention is shown in Figure 1. Figure 1 shows the constitution of a video signal encoding multiplexer of the present invention, and encoded quantity storage circuit 14, channel selecting circuit 15, and transfer encoded quantity calculating circuit 16 are newly installed in the video signal encoding multiplexer of the prior art shown in Figure 13. The same symbols are given to the same parts as those of Figure 13. In addition, the difference is that the read out of encoded data, which are output to the coded data multiplexing circuit from the buffer memory 3 of each channel, is controlled by a control signal from channel selecting circuit 15 instead of the target encoding quantity allocating circuit 9.

[0026]

Figure 2 shows a constitutional example of the newly installed encoded quantity storage circuit 14. In Figure 2, a memory 17 is a FIFO type memory constituted to write 3 kinds of data as one set and to read them out in a written sequence. The memory 17 sequentially stores the encoded amount of the current field input from the encoded quantity counter 6, the time number in which vertical synchronous signals input into the encoded quantity storage circuit 14 are counted and expressed by a counter 19, and the storage address in the buffer memory 3 in which the last encoded data of the encoded data generated in the current field are stored. In addition, a counter 18 counts the number of data sets stored in the memory 17 by adding 1 when data are written into the memory 17 and subtracting 1 when data are read out. Moreover, a temporary storage memory 20 temporary stores one set of the oldest data (time number: t0, amount encoded: g0, end address: b0) read out of the FIFO type memory 17.

[0027]

Next, operation of the video signal encoding multiplexer of the present invention will be further explained with reference to Figures 1-5. In Figure 1, since encoding of several provided video signals and allocating of the target encoding amount are carried out similarly to the device of Figure 13, an explanation of said parts will be omitted. Each encoded quantity storage circuit 14 of each newly installed channel outputs one set of data (t0, g0, b0) in the oldest field stored in the temporary storage memory 20 to the channel selecting circuit 15. The channel selecting circuit 15 compares the time number (t0) of each set of data obtained from the temporary storage memory 20 of the encoded quantity storage circuit 14 of each channel and selects the channel number with the oldest time number. In this case, if several channels have the same time number, the total encoded amount accumulated in the buffer memory 3 is read out of the encoded quantity

counter 6 of the corresponding individual channel and compared, and the channel number with the largest accumulated encoded amount is selected. A selecting signal is then output to the transferred encoded quantity calculating circuit 16 of the channel of the selected channel number (Figure 3 schematically shows a flow chart example of the process of the above-mentioned channel selecting circuit 15).

Moreover, the channel selecting circuit 15, for example, may also be constituted by microcomputers, etc., and can have various other constitutions.

[0028]

The transferred encoded quantity calculating circuit 16 of the corresponding channel, which has received the selecting signal for selecting a channel from the channel selecting circuit 15, compares the encoded amount (g0) of the corresponding field stored in the temporary storage memory 20 of the above-mentioned encoded quantity storage circuit 14 with a preset fixed amount gMAX of encoding and selects a smaller amount encoded as gt = MIN (g0 or gMAX). The transferred encoded quantity calculating circuit 16 then outputs the selected amount encoded gt and an encoded data readout control signal to the buffer memory 3 of the corresponding channel (Figure 4 schematically shows a flow chart example of the process for selecting the amount encoded in the above-mentioned transferred encoded quantity calculating circuit 16). The encoded data of the amount encoded gt read out of the buffer memory 3 by the amount encoded gt and the encoded data readout control signal are sequentially output after adding a code (header) required for transmission in the encoded data multiplexing circuit 10.

[0029]

Next, the transferred encoded quantity calculating circuit 16 outputs the selected amount encoded gt to the buffer memory 3 and also outputs it to the encoded quantity storage circuit 14. The encoded quantity storage circuit 14 attains a value (g0 – gt) in which the amount encoded gt is subtracted from the amount encoded (g0) stored in the temporary storage memory 20 and restores said value instead of the amount encoded (g0) stored up to now into the temporary storage memory 20, when (g0 – gt) > 0. Conversely, when (g0 – gt) = 0, the data of the oldest field are read out of the memory 17 and input into the temporary storage memory 20, and the data in the temporary storage memory 20 of each channel are output to the channel selecting circuit 15. The above-mentioned operation is repeated.

[0030]

States of change in the amount encoded in the buffer memories at the transmission side and the reception side through the above-mentioned series of operations are shown in Figure 5. It

is assumed that one square block indicates the amount encoded gMAX. In the video signal encoding multiplexer of this application example, the encoded data are transmitted from the encoded data with the oldest field number. Therefore, as shown in Figure 5(b), the distribution of effective transmission rates is not directly affected, even if the amount the video signals of the current field encoded increases and decreases. In other words, as shown in Figure 5(c), without immediately increasing the transmission rate of channel a for one field period, unlike the conventional example of Figure 14(c), first, the encoded data of the fourth field of both channels a and b are transmitted. As a result, the coding prior to a scene change stored in the buffer memory at the transmission side is cleared. Therefore, even in Figure 5(f) in which a stationary state is formed after the passage of sufficient time, an unbalance in the number of marginal fields is not generated, unlike [the state illustrated] in Figure 14(f). For this reason, an increase in the number of marginal fields is not required, unlike in the prior art, and transmission delay due to the storage capacity of the buffer memory and the marginal fields can be suppressed to a minimum.

[0031]

As mentioned above, in the video signal encoding multiplexer of the present invention, distortion is not concentrated on only one channel, and the number of marginal fields can be suppressed to a minimum. Therefore, an effective signal encoding multiplexer with a small circuit scale of the buffer memories without useless transmission delay can be obtained. In addition, in the video signal encoding multiplexer of the present invention, a transmission rate corresponding to the amount actually encoded is automatically allocated. For this reason, even if the amount actually encoded is shifted from the target amount of encoding, since the transmission rate allocation is automatically changed and the amount of errors is distributed over several channels, the storage capacity of the buffer memories can be further reduced.

[0032]

Application Example 2

A second application example of the present invention is shown in Figure 6. Figure 6 is a schematic diagram showing an arithmetic flow chart using the transferred encoded quantity circulating circuit 16 of the video signal encoding multiplexer of the present invention as a separate means. The other circuits of the video signal encoding multiplexer and their operations are similar to those of the first application example. The amount transferred and encoded in the transferred encoded quantity calculating circuit 16 in this application example is calculated as follows. The transferred encoded quantity calculating circuit 16 compares the encoded amount (g0) of said field stored in the temporary storage memory 20 of the input encoded quantity

storage circuit 14 (see Figure 2) with a preset fixed amount gMAX of encoding and outputs gt = g0 if g0 < gMAX, and a value gt = gMAX – gMIN in which a preset fixed amount gMIN of encoding is subtracted from gMAX if g0 ≥ gMAX, to the buffer memory 3. The encoded data of the encoded amount gt read out of the buffer memory 3 are sequentially output after adding a code (header) required for the transmission in the encoded data multiplexing circuit 10.

[0033]

In the flow chart of the transferred encoded calculating circuit in the first application example shown in Figure 4, if g0 ≥ gMAX, gt = gMAX. For this reason, in an extreme case, the remaining amount encoded in said field is 1 bit, and in transmitting the next encoded data, a code (header) for the transmission of several tens of bits is added due to the 1 bit before transmitting. Conversely, for the transferred encoded quantity calculating circuit of this application example shown in Figure 6, if gt = gMAX – gMIN is set, the lowest amount gMIN of encoding can be secured in transmitting the next encoded data. In this manner, if the transferred encoded quantity calculating circuit 16 of this application example is used, the inconvenience in which a code (header) for the transmission of several tens of bits must be added to transfer an image code of several bits is not generated, so a good transmission rate distribution can be realized.

[0034]

Application Example 3

A third application example of the present invention is shown in Figure 7. Figure 7 is a schematic diagram showing an arithmetic flow chart using the transferred encoded quantity circulating circuit 16 of the video signal encoding multiplexer of the present invention as a separate means. In addition, in this application example, it is assumed that the buffer memory 3 has a circulatory storage structure. In other words, as schematically shown in Figure 8, a sequential storage from address 0 is started, and when the address reaches the last address B-1 (the storage capacity is assumed to be B), the sequential storage is continued after returning to address 0. In Figure 8, the address br is a starting point of the data stored in the buffer memory 3 and shows the next data readout starting point. Moreover, the address bw shows the starting point of a new data input. The other circuits of the video signal encoding multiplexer and their operations are similar to those of the first application example.

[0035]

In the transferred encoded quantity calculating circuit 16 of this application example, the difference from the first and second application examples is that the encoded amount for reading the encoded data out of the buffer memory 3 is selected by designating the storage address (end

address) in the buffer memory 3 in which the last encoded data of the encoded data to be read out are stored. In other words, the transferred encoded quantity calculating circuit 16 reads the encoding end address (b0) generated in the corresponding field out of the temporary storage memory 20 of the encoded quantity storage circuit 14 or the readout address br as a starting point of the data storage out of the buffer memory 3. An imaginary address b0' (see Figure 8) in an imaginary memory having an infinite storage capacity (a circulatory storage structure) is then attained by the following equation.

$$\text{When } br < b0,\ b0' = b0 \qquad (2)$$
$$\text{When } br > b0,\ b0' = b0 + B$$

[0036]

Next, the imaginary address and the numerical value b'MAX = br + gMAX attained from the separately read address br are compared, and the address bt' in the imaginary memory or the storage address bt in the buffer memory 3 in which the last encoded data of a series of encoded data that are transmitted is stored is attained by the following equation.

$$\text{When } b0' < b'MAX = (br + gMAX),\ bt' = b0' \qquad (3)$$
$$\text{When } b0' > b'MAX,\ bt' = b'MAX - gMIN$$

From the value bt', the address bt of an actual buffer memory is attained by the following equation, and the value is output to the buffer memory 3.

$$\text{When } bt' < B,\ bt = bt' \qquad (4)$$
$$\text{When } bt' > B,\ bt = bt' - B$$

The buffer memory 3 reads the encoded data from the readout start address br to the address bt, adds a code (header) required for transmission in the encoded data multiplexing circuit 10, and sequentially outputs them. As mentioned above, in this application example, since the other circuits and their operations are similar to those of the first application example, effects similar to those of the first or second application example can also be obtained.

[0037]

Application Example 4

A fourth application example of the present invention is shown in Figure 9. Figure 9 shows the constitution of a video signal encoding multiplexer of the present invention. An IP synchronous control circuit 21 is further installed in the video signal encoding multiplexer of the first application example of the present invention. Generally, continuous images of 2 fields or 2 frames in dynamic images are very similar images, and the differential signal (hereinafter, described as P signal) attained by correcting and subtracting the motion of a subject of two images is almost 0. Therefore, if this differential signal is used in encoding, the amount of

encoding can be significantly reduced. However, if only the differential signal is continuously transmitted, if a disturbance is introduced into the transmission system, the subsequent images cannot be reproduced. For this reason, in an ordinary video signal encoder using a differential signal, encoded signals (hereinafter, described as I signals) of video signals of the entire image are transmitted at each fixed field period Fg, and even if a disturbance is introduced, images can be continuously reproduced.

[0038]

In transmitting the encoded data constituted in this manner through the conventional video image encoding multiplexer shown in Figure 13, states of change in the amount encoded in the buffer memories at the transmission side and the reception side are schematically shown in Figure 10. In Figure 10, the third field and the eighth field are I signals, and the other fields are P signals. In this case, since the amount of encoding of two channels a and b is simultaneously increased, a risk state having no marginal field or marginal encoding as part of it at the reception is generated (Figure 10(d)). Therefore, the amount of encoding of the P signal is usually adjusted so that it is slightly smaller than the transmission rate and is gradually restored. However, it is not understood that the marginal field disappears temporarily, and a margin of one field is required. In addition, the restoration of the above-mentioned fixed field period Fg to a normal state requires a long time period.

[0039]

Accordingly, in this application example, an IP synchronous control circuit 21 controlling the transmission timing of the I signals so that the timings of the signals are shifted from each other for each channel has been newly added to the constitution of the video signal encoding multiplexer shown in Figure 1. States of change in the amount of encoding in the buffer memories at the transmission side and the reception side under this control are schematically shown in Figure 11. As shown in Figure 11(d), the marginal field at the reception side is also reduced in this application example. However, encoding of the marginal field does not disappear completely, unlike the reception side of Figure 10(d). Therefore, the amount of encoding of the marginal field to be added is also small, and the increase in the circuit scale of the buffer memories and the transmission delay can be minimized. In addition, a normal state returns at a period of about 1/2 of the case of Figure 10 (in Figure 10, a marginal field is present at the reception side of Figure 10(f), and in Figure 11, a marginal field is present at the reception side of Figure 11(e)), and the degree of risk of generating erroneous operations can be significantly reduced.

[0040]

As a control method of the transmission timing of the I signals in the IP synchronous control circuit 21, for example, the value of the fixed field period Fg of one channel may be temporarily set at a large value of one field or more such as (Fg + 1) and shifted to a target timing position slowly or at one time. In addition, at that time, the value of the fixed field value Fg may be set at a small value, but the amount of encoding is similarly temporarily increased. As mentioned above, in the video signal encoding multiplexer of this application example, in addition to effects similar to those of the first application example, the marginal field shortage at the reception side due to the increase in the amount of encoding of the I signals is minimized, so that a video signal encoding multiplexer with a small circuit scale of buffer memories without a useless transmission delay can be obtained.

[0041]

Moreover, as the time number used in each of the above-mentioned application examples, a sufficiently large number F (field) may be prepared and used in a circulatory fashion. In other words, counting of the field number starts from 0, and the time number is provided so that when the number exceeds the set F, it returns to 0. When the preset number is F0 and two time numbers are f1 and f2, the age of the time numbers may be discriminated by the following expression.

When $|f1 - f2| \leq F0$, time number with a small numeral of f1 and f2

When $|f1 - f2| > F0$, time number with a large numeral of f1 and f2 (5)

The number F can be arbitrarily set as long as it is (2F0 + 1) or more. However, in the method of the present invention, in principle, the difference in field time numbers to be compared with each other is not separated by ± 1 or more. For this reason, F0 can be set at an arbitrary numeral of 1 or more, and F may be set so that a numeral of 3 or more can be counted.

[0042]

Furthermore, in the encoded quantity storage circuit shown in Figure 2, the encoded amount (g0) of the field and the last storage address (b0) of the field encoding have been stored in the memory 17. However, only the last storage address (b0) may be stored, and the encoded amount (g0) of the field may be attained from the difference in the storage address of two continuous fields. In addition, when only the encoded amount (g0) is used and selected as in the second application example, it is apparent that only the encoded amount (g0) may also be stored. Moreover, the last storage number (b0) of the field encoding has been stored in the memory 17, but it is apparent that the start address of the encoding may also be stored.

[0043]

Furthermore, in the encoded quantity storage circuit shown in Figure 2, since a FIFO type memory in which the stored content is erased if data are read out has been used as the memory 17, the temporary storage memory 20 for temporarily storing the read data has also been used. However, if a memory (for example, RAM) of a type in which the stored content is not erased even by reading and data are read out many times is used as the memory 17, it is apparent that g0 and other data may be directly read out of the memory 17. In addition, in the transferred encoded quantity calculating circuit 16 of each of the above-mentioned application examples, g0 and gMAX have been compared, and the encoding amount gt for transmitting a smaller value has been selected. However, it is apparent that gt = g0 (corresponding to setting of gMAX to a sufficiently large value) may always be set.

[0044]

Moreover, if one set of data of a new field stored in the memory 17 shown in Figure 2 is read, and the numeral of the counter 18 is 0, that is, if encoding of the next field has not been completed and the value of the encoded quantity counter 6 does not extend beyond a fixed amount such as gMIN and gMAX, preferably, a time number (for example, F + 1) showing that there is no encoded data to be transmitted is stored in the temporary storage memory 20, so selection in the channel selecting circuit 15 is excluded. In this manner, erroneous operations in which readout of encoded data in the buffer memory 3 is started in spite of the absence of encoded data to be transmitted can be prevented.

[0045]

Furthermore, in each of the above-mentioned application examples, the amount encoded for the previous prescribed period has been explained using a case in which the amount encoded is arranged at a general field unit, but as the prescribed period, it is apparent that an optional prescribed period such as 1 of an integer portion of a field, not to mention a frame unit may also be set and is included in the scope of protection of the present invention. In addition, as mentioned above, for example, if the prescribed period is 1 of an integer portion of a field, since an optional time can be set apart from synchronous signals such as vertical synchronous signals of each channel, video signals of several asynchronous channels can be multiplexed and transmitted. Moreover, the amount of encoding in each of the above-mentioned application examples is not necessarily required to be a bit unit. For example, it is apparent that a value showing bytes, words, or an arbitrary number of bits as a unit may also be used. However, in this case, there is a possibility that a shortage will result in the last encoding unit of a field. For this

reason, clearly, a completed encoding unit must be formed by filling the shortage portion with dummy codes or part of the codes of the next field.

[0046]

Furthermore, in Figure 1, an encoded quantity storage circuit 14 and a transferred encoded quantity calculating circuit 16 have been installed for each channel. However, it is apparent that at least one circuit including them may be arranged as one unit to control the centralization. In addition, in each of the above-mentioned each application examples, a maximum encoding amount gMAX for transmission at one time has been set, but without installing this limitation, it is apparent that the encoded data may be transmitted at a unit of one field.

[0047]

Effect of the invention

As explained, in the video signal encoding multiplexer of the present invention, since encoded data are always sequentially transmitted from the encoded data with the oldest field, distortion is not concentrated on only one channel. For this reason, the number of marginal fields can be suppressed to a minimum, so a good video signal encoding multiplexer with a small circuit scale of buffer memories without a useless transmission delay can be obtained. In addition, since a transmission rate corresponding to the amount actually encoded is automatically allocated, even if the amount actually encoded is shifted from a target amount of encoding, since the transmission rate allocation is automatically changed and the amount of errors is distributed to several channels, the storage capacity of the buffer memories can be further reduced.

Brief description of the figures

Figure 1 is a constitutional diagram showing the video signal encoding multiplexer of a first application example of the present invention.

Figure 2 is a constitutional diagram showing an encoded quantity storage circuit of the present invention.

Figure 3 is an arithmetic flow chart showing a channel selecting circuit of the present invention.

Figure 4 is an arithmetic flow chart showing a transferred encoded quantity calculating circuit of the present invention.

Figure 5 is an illustrative diagram showing changes in the encoded amount stored in the first application example of the present invention.

Figure 6 is an arithmetic flow chart showing a transferred encoded quantity circulating circuit of a second application example of the present invention.

Figure 7 is an arithmetic flow chart showing a transferred encoded quantity circulating circuit of a third application example of the present invention.

Figure 8 is a schematic diagram showing a buffer memory structure for circulatory storage

Figure 9 is a constitutional diagram showing the video signal encoding multiplexer of a fourth application example of the present invention.

Figure 10 is an illustrative diagram showing changes in the encoded amount stored in a conventional video signal encoding multiplexer.

Figure 11 is an illustrative diagram showing changes in the encoded amount stored in the video signal encoding multiplexer of the fourth application example of the present invention.

Figure 12 is a constitutional diagram showing a conventional video signal encoder.

Figure 13 is a constitutional diagram showing a conventional video signal encoding multiplexer.

Figure 14 is an illustrative diagram showing changes in the encoded amount stored in the conventional video signal encoding multiplexer.

Explanation of the reference symbols

2 Encoding circuit
3 Buffer memory
5 Complexity calculating circuit
6 Encoded quantity counter
7 Quantization step calculating circuit
9 Target encoding amount allocating circuit
10 Encoded data multiplexing circuit
14 Encoded quantity storage circuit
15 Channel selecting circuit
16 Transferred encoded quantity calculating circuit
17 Memory
18 Counter
19 Counter
20 Temporary storage memory
21 IP synchronous control circuit

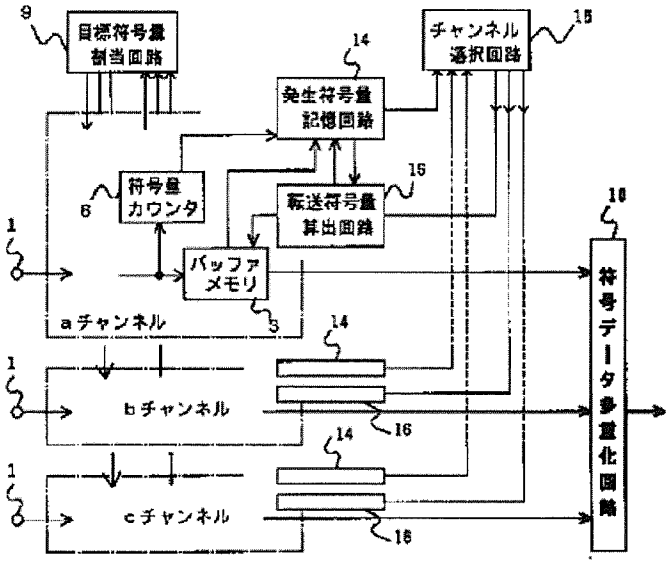

Figure 1

Key: a Channel
b Channel
c Channel
3 Buffer memory
6 Encoded quantity counter
9 Target encoding quantity allocating circuit
10 Encoded data multiplexing circuit
14 Encoded quantity storage circuit
15 Channel selecting circuit
16 Transferred encoded quantity calculating circuit

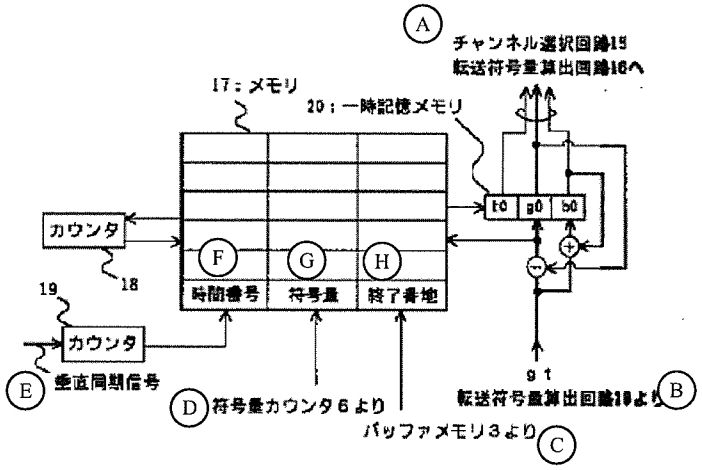

Figure 2

Key: 17 Memory
18 Counter

19 Counter
20 Temporary storage memory
A To channel selecting circuit 15 and transferred encoded quantity calculating circuit 16
B From transferred encoded quantity calculating circuit 16
C From buffer memory 3
D From encoded quantity counter 6
E Vertical synchronous signal
F Time number
G Amount encoded
H End address

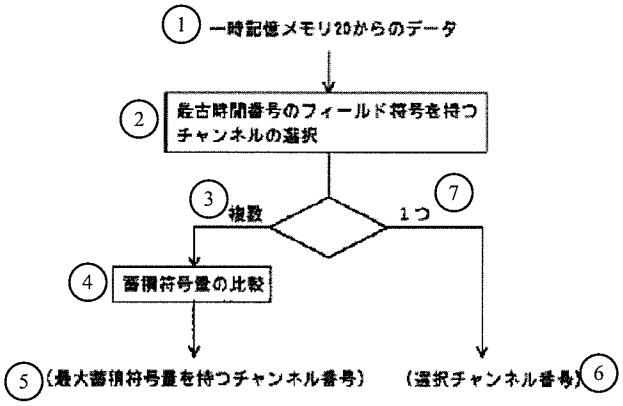

Figure 3

Key: 1 Data from temporary storage memory 20
2 Selection of a channel having field encoding with the oldest time number
3 Several
4 Comparison of the encoded amount stored
5 Channel number having the largest encoded amount stored
6 Selected channel number
7 One

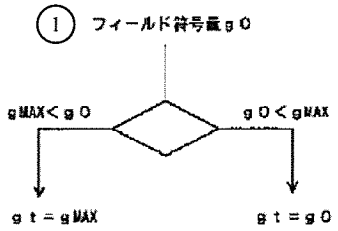

Figure 4

Key: 1 Encoded amount g0 of field

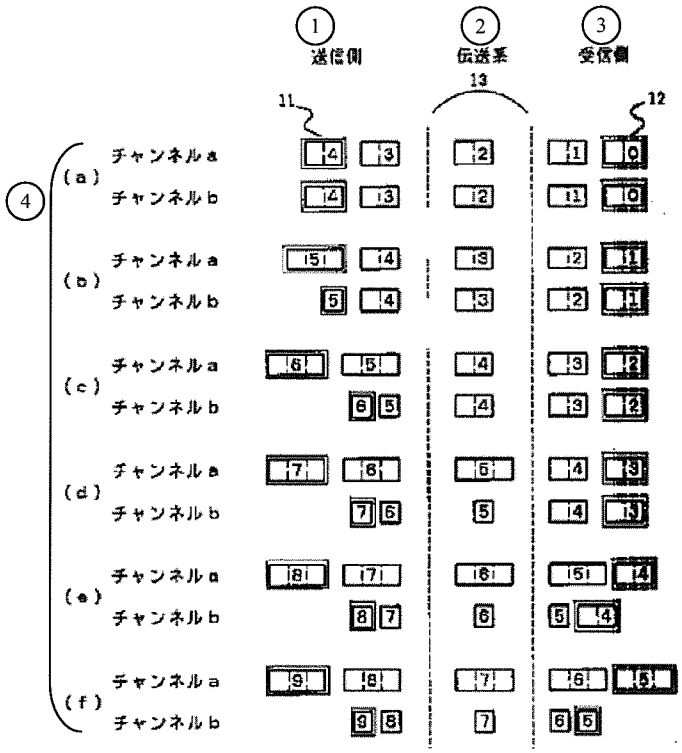

Figure 5

Key: 1 Transmission side
2 Transmission system
3 Reception side
4 Channel a
Channel b

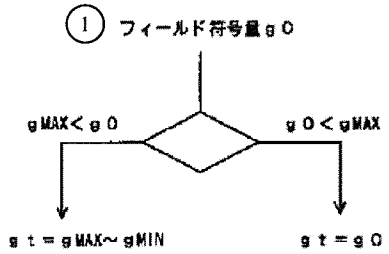

Figure 6

Key: 1 Encoded amount g0 of field

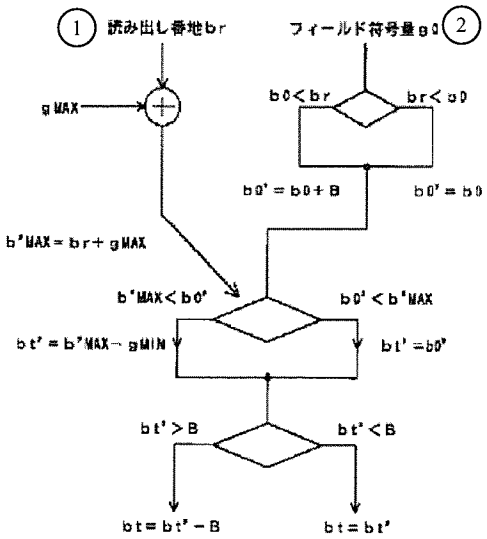

Figure 7

Key: 1 Readout address br
2 Encoded amount g0 of field

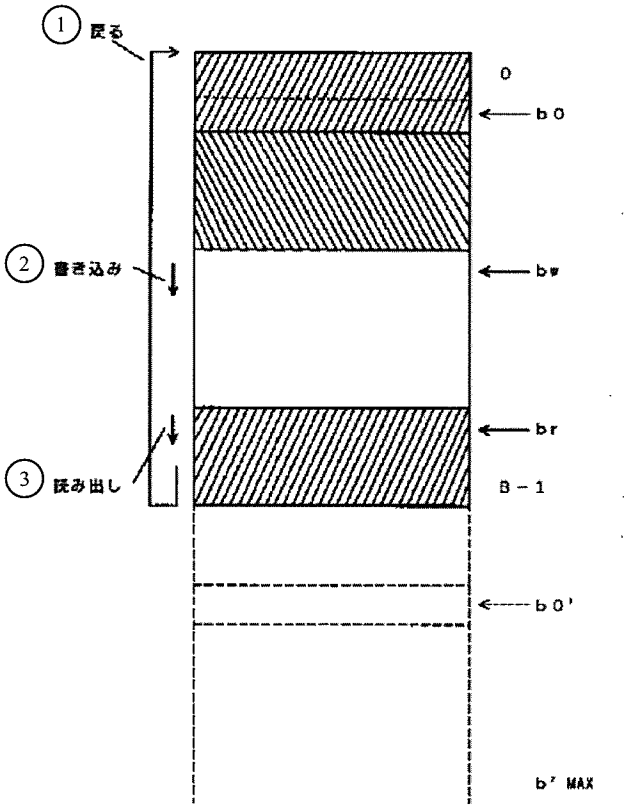

Figure 8

Key: 1 Return
2 Write
3 Readout

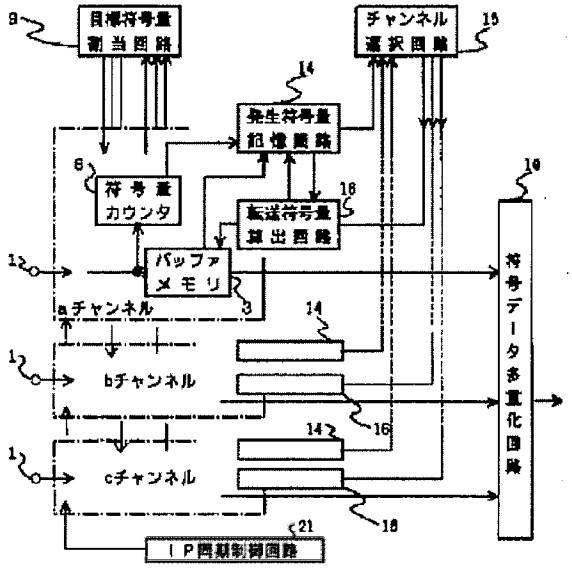

Figure 9

Key:
- a Channel
- b Channel
- c Channel
- 3 Buffer memory
- 6 Encoded quantity counter
- 9 Target encoding quantity allocating circuit
- 10 Encoded data multiplexing circuit
- 14 Encoded quantity storage circuit
- 15 Channel selecting circuit
- 16 Transferred encoded quantity calculating circuit
- 21 IP synchronous control circuit

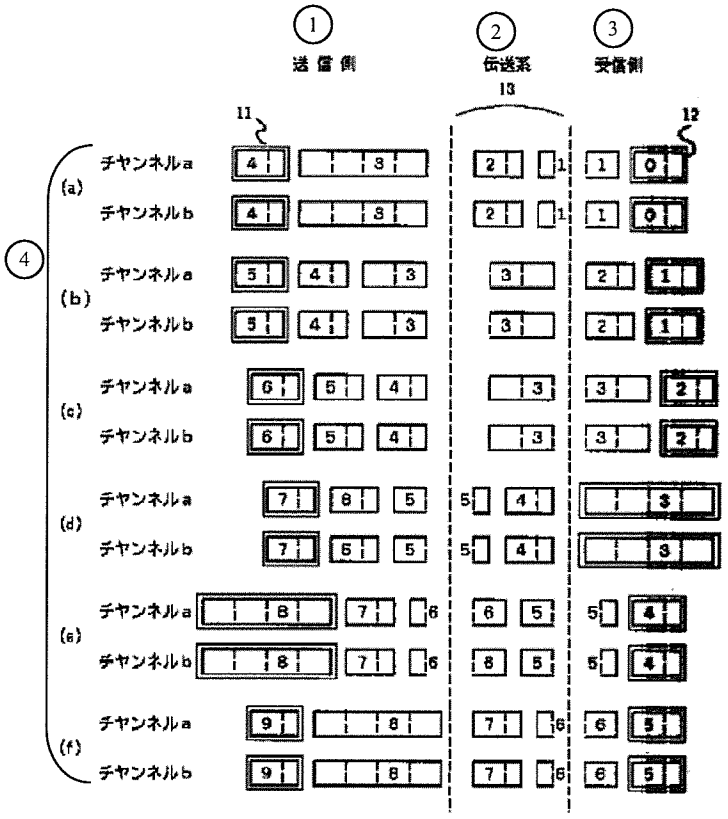

Figure 10

Key: 1 Transmission side
2 Transmission system
3 Reception side
4 Channel a
Channel b

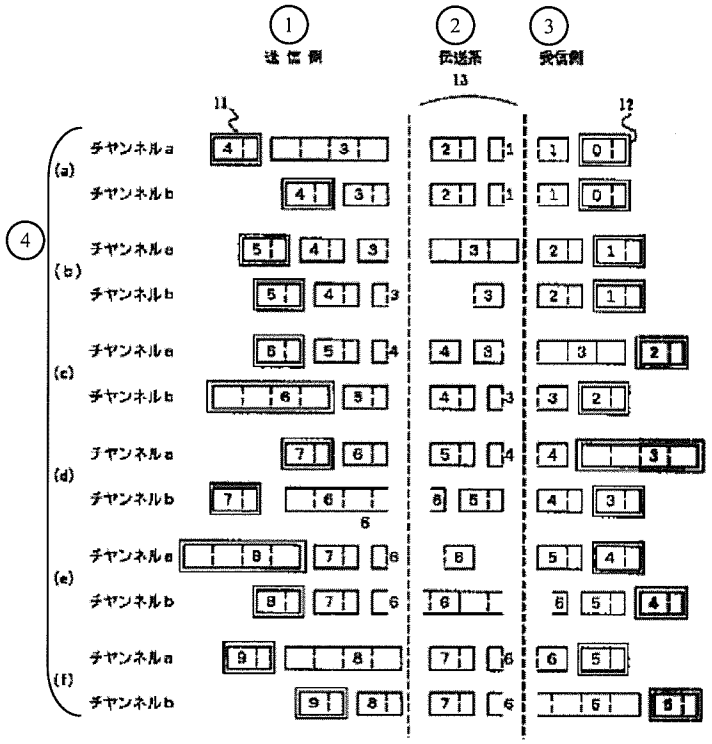

Figure 11

Key: 1 Transmission side
2 Transmission system
3 Reception side
4 Channel a
Channel b

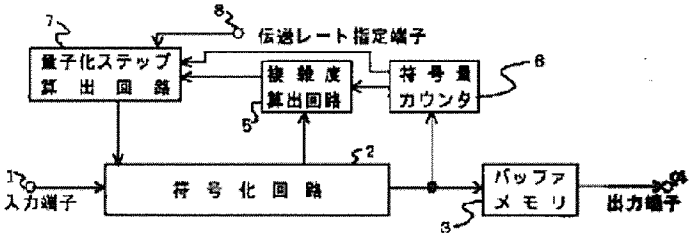

Figure 12

Key: 1 Input terminal
2 Encoding circuit
3 Buffer memory
4 Output terminal
5 Complexity calculating circuit
6 Encoded quantity counter
7 Quantization step calculating circuit
8 Transmission rate designating terminal

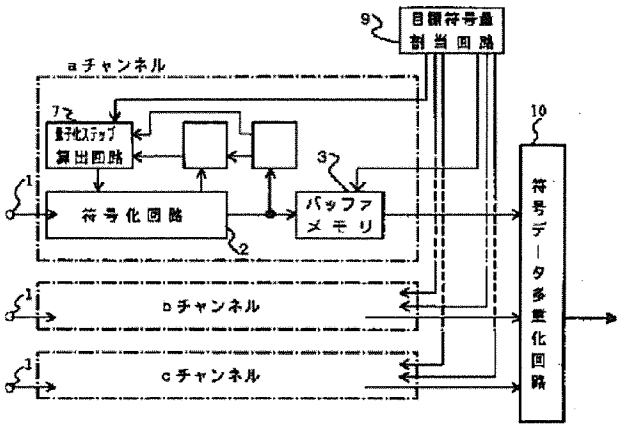

Figure 13

Key:
- a Channel
- b Channel
- c Channel
- 2 Encoding circuit
- 3 Buffer memory
- 7 Quantization step calculating circuit
- 9 Target encoding quantity allocating circuit
- 10 Encoded data multiplexing circuit

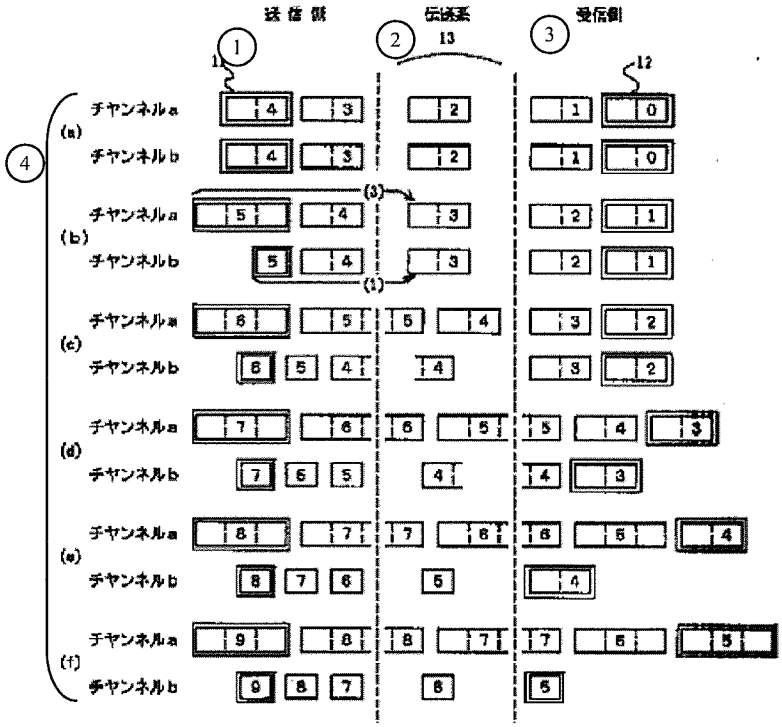

Figure 14

Key: 1 Transmission side
2 Transmission system
3 Reception side
4 Channel a
Channel b

Continued from front page

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